REMARKS

This is a full and timely response to the outstanding non-final office action mailed July 24, 2008. Reconsideration and allowance of the application and pending claims are respectfully requested.

Claim Amendments:

Independent claims 1, 11, 21, and 32 have been amended.

Claims 4, 14, and 24 have been canceled.

New claim 35 has been added reciting subject matter similar to that of claim 11.

Subject matter of the canceled claims has been added to the above independent claims.

Various other claims are amended as indicated in the previous pages.

Claim Rejections – 35 U.S.C. §103(a)

The Examiner at page 2 of the Office Action rejected claims 1-4, 8-14, 18-24, and 28-34 under 35 U.S.C. §103(a) as being unpatentable over Horowitz et al. (US Patent 7,142,612) in view of Svensson "IEEE Journal of solid-state circuits: A 3-level Asynchronous Protocol for a differential Two-Wire communication link".

The Examiner at page 11 of the Office Action rejected claims 5-7, 15-17, and 25-27 under 35 U.S.C. §103(a) as being unpatentable over Horowitz et al. (US Patent 7,142,612) in view of Svensson "IEEE Journal of solid-state circuits: A 3-level Asynchronous Protocol for a differential Two-Wire communication link" and Huang et al. (US Patent 5,798,535). This rejection is respectfully traversed below.

The Examiner at pages 3, 5, 7, and 9 of the Office Action agrees that Horowitz et al. does not teach "a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods" as recited in claim 1 but asserted that Svensson makes obvious this element.

In an exemplary embodiment of the invention, the application in hand is directed to at least one port includes a multi-level analog signaling circuit arrangement that includes a

transmitter to encode data bits represented by multi-level analog signals. A data communications bus that couples the transmitter to a receiver in another port includes at least two multi-level signal buses (either differential or single-ended) for conveying the encoded data bits such that, on each multi-level signal bus, during each data bit period the signal level is required to change from a first signal level to a second, different signal level. The transmitter indicates a data boundary, such as the beginning or the end of multi-bit frame, to the receiver by holding one of the multi-level signal buses of the at least two multi-level signal buses at the same level for at least two consecutive bit periods.

Svensson is directed to a differential two-wire communication link with a 3-level asynchronous protocol. The proposed 3-level code carrying both data and clock contains three differential states (0, 1), (1, 0), and (0, 0). Data is encoded and transmitted by a differential driver and received by two identical comparators with a designed systematic offset (page 1132, section V "Conclusion", right column, paragraphs 1 and 2). Fig. 6 discloses that from the codes received, the clock can be extracted from their OR results (or NOR results), as long as half of them are reversed by a control signal. The task is to detect the borders where the OR results should be reversed and to create the control signal. An edge-triggered flip-flop connected in a divide-by-two circuit mode can be used to produce the control signal (pages 1130-1131, section B "Clock Extractor", left column, paragraph 1). Svensson does not disclose a start or an end of a multi-bit frame. Svensson cannot be seen to make it obvious, indicating a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods, wherein the data boundary comprises one of *a start or an end* of a multi-bit frame as recited now in claim 1. Svensson discloses the most straight and efficient design of the encoder is to use a **bi-directional register ring which consists of three registers** (page 1130, section A "Encoder and Driver", right column, paragraph 1). Svensson discloses an edge-triggered flip-flop, a bi-directional register ring but Svensson cannot be seen to disclose or make it obvious the data boundary comprises one of a *start or an end* of a multi-bit frame.

Further, Svensson does not make it obvious to indicate a data boundary to the receiver by *holding* one of the multi-level signal buses at the same level for at least two consecutive bit periods as recited in claim 1. In every instance, Svensson's borders are indicated by a change to

one of the state machine bits C_1 or C_2. This must necessarily hold true by Svensson because the state machine uses flip flops, and a border is only indicated when a clock is extracted, which can only happen at a change in output from the flip flops (page 1131, the paragraph spanning both columns). If a signal O_1 or O_2 of Svensson were held steady for two consecutive bit periods as the rejections of claims 4, 14 and 24 asserts, not only could Svensson not extract a clock at that time but the absence of changing C_1 or C_2 in the state machine requires that Svensson conclude there is no border, whether of a frame or otherwise. For every instance in which Svensson can extract a clock from C_1 or C_2, that clock is indicated by a change to C_1 or C_2. If one of C_1 or C_2 were held steady while the other were changed, the extracted clock would be indicated by the changed one of C_1 or C_2; the other one which was held steady would indicate nothing whatsoever in Svensson. Svensson is therefore seen to teach exactly the opposite of the independent claims as amended herein with the subject matter of claims 4, 14 and 24.

Based on the above explanations and arguments, it is respectfully submitted that the asserted combination of Svensson and Horowitz et al. cannot be seen to render obvious claim 1 as amended herein with the subject matter of claim 4. The Applicant respectfully asserts that as claims 2-3, and 5-10 are dependent on claim 1 they should be allowable at least for that dependency.

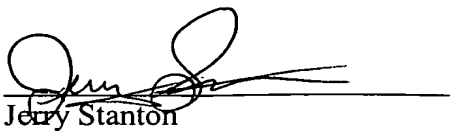
Independent claims 11, 21, and 32 which are amended similarly to claim 1 in relevant respects, also distinguishes over the references for the reasons detailed above and should be allowed. The Applicant respectfully asserts that as claims 12-13, and 15-20 depend on claim 11, claims 22-23, and 25-31 depend on claim 21, and claims 33-34 depend on claim 32 they should be allowable at least for that dependency.

New claim 35 is similar in relevant respects to claim 11 but reciting in means language. For reasons stated above with respect to claim 1, claim 35 is seen to be in condition for allowance.

The Applicant respectfully requests that all the rejections be withdrawn and that all pending claims now be passed to issue. The undersigned representative welcomes the

opportunity to address any matters that may remain via teleconference in order to move this application to issue.

Respectfully submitted:



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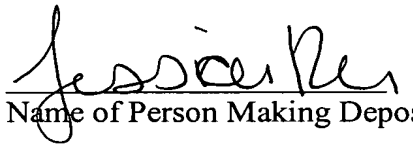

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